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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/562,303	12/22/2005	Axel Andersch	2003P08945WOUS	3763

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EXAMINER	
THANGAVELU, KANDASAMY	
ART UNIT	**PAPER NUMBER**
2123	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/562,303	ANDERSCH ET AL.	
	Examiner	Art Unit	
	KANDASAMY THANGAVELU	2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 December 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *23-32* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *23-25 and 28-30* is/are rejected.

7)☒ Claim(s) *26,27,31 and 32* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *22 December 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This communication is in response to the Applicants' Amendment dated December 17, 2008. Claims 12-22 were canceled. Claims 23-32 were added. Claims 23-32 of the application are pending. This office action is made final.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains.

3. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

4. Claims 23-25 and 28-30 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Hollander** (U.S. Patent Application 2002/0073375) in view of **Mc Connell et al.** (U.S. Patent Application 2001/0049593), and further in view of **Sano et al.** (U.S. Patent 5,991,533).

4.1 **Hollander** teaches method and apparatus for test generation during circuit design. Specifically, as per claim 28, **Hollander** teaches a system for combining and representing signals of a hardware simulation device (Abstract, L1-2; Page 2, Para 0031, L1-2; Page 2, Para 0035; Page 3, Para 0050; Fig. 3; Page 5, Para 0091; Page 6, Para 0101) and elements of a listing of a software program (Page 2, Para 0031, L5; Para 0032 to Para 0034; Page 4, Para 0066; Page 6, Para 0103, L2-8, comprising:

a software program having program code stored in a memory of a circuit; and a program list file from the software program comprising a list of elements representing the sequence of the software program, wherein the elements comprise program commands and any associated comments (Page 2, Para 0031, L4-5; Para 0032 to Para 0034; Para 0036; Fig. 7; Page 5, Para 0091 and Para 0092; Fig. 5, Item 163);

a hardware simulation device for running a hardware simulation of the circuit (Page 2, Para 0035; page 6, Para 0101) described in a hardware description language (HDL) (Page 1, Para 0010, L1-6; Page 2, Para 0035; Page 5, Para 0094, L1-2; Page 6, Para 0103, L1-2) in accordance with an input data file compiled from the software program as simulation code (Page 1, Para 0010, L6-7; Page 7, Para 0127, L1-2) to obtain output signals (Page 1, Para 0010, L7-9; page 5, Para 0095, L3 to Page 6, Para 0095, L5);

a debugger for receiving the output signals from the hardware simulation (Abstract, L22-23; Page 1, Para 0010, L5-9) and the elements from the program list file (Abstract, L22-25; Page 3, Para 0050, L1-2; Page 6, Para 0103, L2-8; Page 6, Para 0109, L3-5; Page 8, Para 0152) and coupling output signals and elements that correspond(abstract, L22-25; Page 3, Para 0050, L1-2); and

a graphical display for displaying a combined representation of the output signals and the elements Abstract, L22-25; Page 5, Para 0094, L4-6; Page 6, Para 0103, L8-9; Page 8, Para 0151), comprising a first area for displaying the list of elements representing the sequence of the software program (Fig 7; Page 6, Para 0103, L8-9; Page 8, Para 0152 to Para 0155) and a second area for displaying the output signals from the hardware simulation (Page 5, Para 0095, L3 to Page 6, Para 0095, L5; Page 6, Para 0103, L8-9; Page 8, Para 0151).

Hollander teaches running the hardware simulation and running the external software on the hardware simulation (Page 6, Para 0103). **Hollander** does not expressly teach a marking unit for synchronizing a first visual marking of a selected element in the first area with a second visual marking of a corresponding output signal in the second area based on the coupling by the debugger. **Mc Connell et al.** teaches a marking unit for synchronizing a first visual marking of a selected element in the first area (Abstract, L1-10; Fig. 2 and Fig. 3; Page 6, Para 0074, L1-6 and L13-16; Page 6, Para 0081; Para 0082). It would have been obvious to one of ordinary skill in the art at the time of Applicant's invention to modify the system of **Hollander** with the system of **Mc Connell et al.** that included a marking unit for synchronizing a first visual marking of a selected element in the first area, because that would allow the problems typically encountered during system integration to be solved much earlier in the design cycle, resulting in a shorter design cycle (Page 4, Para 0052, L6-8); and combining the software development with logic simulation results in high performance co-verification ahead of final solution (Page 6, Para 0075, L13-16); and since the hardware and software are designed and debugged together, the

likelihood of getting the design that works the first time is greatly increased (Page 7, Para 0083, L1-4).

Hollander and **Mc Connell et al.** do not expressly teach a second visual marking of a corresponding output signal in the second area based on the coupling by the debugger. **Sano et al.** teaches a second visual marking of a corresponding output signal in the second area based on the coupling by the debugger (Fig. 20; Fig. 22; CL11, L51-61; Fig. 46). It would have been obvious to one of ordinary skill in the art at the time of Applicant's invention to modify the system of **Hollander** and **Mc Connell et al.** with the system of **Sano et al.** that included a second visual marking of a corresponding output signal in the second area based on the coupling by the debugger, because that would enhance the efficiency of development of the CPU circuit and the control system (Abstract, L27-29).

Per Claim 29: **Hollander** and **Mc Connell et al.** do not expressly teach that the graphical display further comprises a third display area for displaying at least a part of the output signals. **Sano et al.** teaches that the graphical display further comprises a third display area for displaying at least a part of the output signals (Fig. 22; CL11, L51-61).

Per Claim 30: **Hollander** teaches that the output signals displayed in the second area comprise waveforms (Page 5, Para 0094, L4-5; Para 0095, L3 to Page 6, Para 0095, L5; Page 6, Para 0103, L8-9; Page 8, Para 0151). **Hollander** and **Mc Connell et al.** do not expressly teach that the graphical display further comprises a third display area for displaying at least a part of

the output signals. **Sano et al.** teaches that the output signals displayed in the third area comprise register values (Fig. 22; CL11, L51-61).

4.2 As per Claims 23-25, these are rejected based on the same reasoning as Claims 28-30, supra. Claims 23-25 are method claims reciting the same limitations as Claims 28-30, as taught throughout by **Hollander, Mc Connell et al.** and **Sano et al.**

Allowable Subject Matter

5. Claims 26-27 and 31-32 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

6. Applicants' arguments filed on December 17, 2008 have been fully considered. Applicants' arguments with respect to art rejection s under 35 USC 103 (a) are moot in view of the applicants' cancellation of all previous claims. The Examiner has used new art against the newly submitted claims.

6.1 As per the applicants' argument that "the art does not show the unique arrangement that produces unique dual kind of display between the hardware simulation output signals and the elements of the program listing with visual synchronized marking between the element of the

software program listing and the corresponding hardware simulation output signals", the examiner has used new references, by **Hollander, Mc Connell et al.** and **Sano et al.**

Hollander teaches a debugger for receiving the output signals from the hardware simulation (Abstract, L22-23; Page 1, Para 0010, L5-9) and the elements from the program list file (Abstract, L22-25; Page 3, Para 0050, L1-2; Page 6, Para 0103, L2-8; Page 6, Para 0109, L3-5; Page 8, Para 0152) and coupling output signals and elements that correspond(abstract, L22-25; Page 3, Para 0050, L1-2); and

a graphical display for displaying a combined representation of the output signals and the elements Abstract, L22-25; Page 5, Para 0094, L4-6; Page 6, Para 0103, L8-9; Page 8, Para 0151), comprising a first area for displaying the list of elements representing the sequence of the software program (Fig 7; Page 6, Para 0103, L8-9; Page 8, Para 0152 to Para 0155) and a second area for displaying the output signals from the hardware simulation (Page 5, Para 0095, L3 to Page 6, Para 0095, L5; Page 6, Para 0103, L8-9; Page 8, Para 0151).

Hollander does not expressly teach a marking unit for synchronizing a first visual marking of a selected element in the first area with a second visual marking of a corresponding output signal in the second area based on the coupling by the debugger. **Mc Connell et al.** teaches a marking unit for synchronizing a first visual marking of a selected element in the first area (Abstract, L1-10; Fig. 2 and Fig. 3; Page 6, Para 0074, L1-6 and L13-16; Page 6, Para 0081; Para 0082).

Hollander and **Mc Connell et al.** do not expressly teach a second visual marking of a corresponding output signal in the second area based on the coupling by the debugger. **Sano et al.** teaches a second visual marking of a corresponding output signal in the second area based on the coupling by the debugger (Fig. 20; Fig. 22; CL11, L51-61; Fig. 46).

ACTION IS FINAL

7. Applicant's amendments necessitated new ground of rejection included in this Office Action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Conclusion

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dr. Kandasamy Thangavelu whose telephone number is

571-272-3717. The examiner can normally be reached on Monday through Friday from 8:00 AM to 5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Paul Rodriguez, can be reached on 571-272-3753. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to TC 2100 Group receptionist: 571-272-2100.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

K. Thangavelu
Examiner, Art Unit 2123
March 7, 2009

/Paul L Rodriguez/
Supervisory Patent Examiner, Art Unit 2123